UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	P99,0401
First Named Inventor or Application Identifier	
Takahisa Ueno et al,	
Express Mail Label No:	

ADDRESS TO: **Assistant Commissioner for Patents**
Box Patent Application
Washington, DC 20231

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

1. X Specification [Total Pages 38]
2. X Drawing(s) (35USC 113) [Total Pages 17]
3. X Declaration and Power of Attorney [Total Pages 3]

a. __ Newly executed declaration (Original copy)

b. __ Copy from prior application (37CFR 1.63(d))
(for continuation/divisional with Box 14 completed)

[Note Box 4 Below]

i. __ DELETION OF INVENTOR(S)
Signed statement attached deleting Inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).

4. __ Incorporation By Reference (usable if Box 3b is checked)
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 3b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

ACCOMPANYING APPLICATION PARTS

5. __ Assignment Papers (cover sheet & documentation)
_____

6. X Letter under 37 CFR 1.41(c).

7. __ English Translation Document *(if applicable)*

8. __ Information Disclosure Statement (IDS)/PTO-1449 __ Copies of IDS Citations

9. X Preliminary Amendment

10. X Return Receipt Postcard (MPEP 503)
(Should be specifically itemized)

11. __ Small Entity Statement(s) (Faxed copy of original) __ Statement filed in prior application, Status still proper and desired

12. X Certified Copy of Priority Document(s) Japanese Aplication No. P10-159050 filed June 8, 1998

13. __ Other:

14. If a CONTINUING APPLICATION, *check appropriate box and supply the requisite information:*

__ Continuation __ Divisional __ Continuation-in-part (CIP) __ of prior application No: __/

CLAIMS AS FILED

(1) FOR	(2) NUMBER FILED	(3) NUMBER EXTRA	(4) RATE	(5) BASIC FEE $760 00
TOTAL CLAIMS 20	15			
INDEPENDENT CLAIMS 3	3			
	ANY MULTIPLE DEPENDENT CLAIMS? ()YES (X) NO			
			TOTAL FILING FEE ->	$760.00

X The Commissioner is hereby authorized to charge any additional fees which may be required in connection with this application, or credit any overpayment to ACCOUNT NO. 08-2290. A duplicate copy of this sheet is enclosed.

X A check in the amount of $ 760.00 to cover the filing fee is enclosed.

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June 7, 1999

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Re: Our Case No. P99,0401
Inventor: Takahisa Ueno et al.
For: SOLID-STATE IMAGING ELEMENT, METHOD FOR DRIVING THE SAME, AND CAMERA SYSTEM

S I R:

Under the provisions of 37 CFR 1.41(c), I am filing the attached application 15 claims, Figures 1-18 on 17 sheets and $760.00 filing fee on behalf of

Takahisa Ueno, Kazuya Yonemoto, Ryoji Suzuki and Koichi Shiono

and request that the application be assigned a Serial Number and filing date pursuant to the provisions of 37 CFR 1.53(b) and 37 CFR 1.53(d).

Respectfully submitted,

John D. Simpson (Reg. No. 19,842)
FOR THE FIRM

491/1077
Enclosures

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

PRELIMINARY AMENDMENT ACCOMPANYING APPLICATION

APPLICANTS:	Takahisa Ueno et al.	ATTORNEY DOCKET NO.: P99,0401
SERIAL NO:		
FILED:	(Filed concurrently herewith)	
INVENTION:	SOLID-STATE IMAGING ELEMENT, METHOD FOR DRIVING THE SAME, AND CAMERA SYSTEM	

Assistant Commissioner of Patents
and Trademarks
Washington, D.C. 20231

S I R:

Between the title and the heading "Background of the Invention" on page 1, insert the following:

--RELATED APPLICATION DATA

The present application claims priority to Japanese Application No. P10-159050 filed June 8, 1998, which application is incorporated herein by reference to the extent permitted by law.--

Respectfully submitted,

(Reg. No. 19,842)

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SOLID-STATE IMAGING ELEMENT, METHOD FOR DRIVING THE SAME, AND CAMERA SYSTEM

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a solid-state imaging element, a method for driving it, and a camera system, and particularly to an amplification type solid-state imaging element such as a CMOS image sensor having an amplification function for each of unit pixels arranged in a matrix form, a method for driving it, and a camera system using amplification type solid-state imaging elements as imaging devices.

2. Description of Related Art

Amplification type solid-state imaging elements, for example, CMOS image sensors have various pixel structures. As an example, there is known a pixel structure having floating diffusion (FD) inside pixels. This pixel structure is advantageous in that sensitivity can be increased because signals are amplified by the floating diffusion. Fig. 18 shows a prior art pixel structure of this type.

In Fig. 18, each of unit pixels 100 arranged in a matrix form includes photogate 101, transfer switch

102, floating diffusion 103, reset transistor 104, amplifying transistor 105, and vertical selection transistor 106. In response to a vertical selection pulse afforded via the vertical selection line 111, the vertical selection transistor 106 selects unit pixels 100 in units of rows, whereby a signal amplified by the amplifying transistor 105 is output to the vertical signal line 112.

By the way, to reduce pixel size requires that the number of elements to constitute a unit pixel 100 is reduced. However, since the pixel structure of a prior art CMOS image sensor described above dictates that three transistors, reset transistor 104, amplifying transistor 105, and vertical selection transistor 106, are used to select the potential of floating diffusion 103 in units of rows for output to vertical signal line 112, a large number of elements are used, hindering reduction of pixel size.

SUMMARY OF THE INVENTION

The present invention has been made in consideration of the above problem and an object of the present invention is to reduce the number of elements making up a unit pixel and offer a solid-state imaging

element having made reduction of pixel size possible, a method for driving it, and a camera system.

A solid-state imaging element according to the present invention comprises:

unit pixels, arranged in a matrix form, which have photoelectric transfer elements, transfer switches for transferring charges stored in the photoelectric transfer elements, charge store parts for storing charges transferred by the transfer switches, reset switches for resetting the charge store parts, and amplifying elements for outputting signals in accordance with the potential of the charge store parts to vertical signal lines;

a vertical scanning circuit for selecting pixels in units of rows by controlling a reset potential afforded to the reset switch;

a horizontal scanning circuit for sequentially selecting signals output to the vertical signal lines in units of columns; and

an output circuit for outputting signals selected by the horizontal scanning circuit via horizontal signal lines.

In a solid-state imaging element of the above configuration, by setting a reset potential afforded to

a reset switch in a unit pixel to, e.g., 0 V at the time of other than pixel selection, the potential of a charge store part becomes Low. By affording, e.g., a pixel source voltage to the reset switch as a reset potential, pixels are selected, and upon the occurrence of a reset pulse, the potential of the charge store part is reset to the pixel source voltage. Namely, by controlling a reset potential, the potential of the charge store part is controlled. Subsequently, signal charges stored in the photoelectric transfer element are transferred to the charge store part and the potential of the charge store part that changes in accordance with the transfer is read into a vertical signal line by an amplifying element.

A method for driving a solid-state imaging element according to the present invention, in a solid-state imaging element comprising unit pixels, arranged in a matrix form, which have photoelectric transfer elements, transfer switches for transferring charges stored in the photoelectric transfer elements, charge store parts for storing charges transferred by the transfer switches, reset switches for resetting the charge store parts, and amplifying elements for outputting signals in accordance with the potential of

the charge store parts to vertical signal lines, selects pixels in units of rows by controlling a reset potential afforded to the reset switches.

In a solid-state imaging element having an amplification function for each pixel, the potential of a charge store part is controlled by controlling a reset potential afforded to a reset switch to reset the charge store part. Thereby, pixels are selected in units of rows without providing an element for vertical (row) selection. That is, the reset switch also has a function to select pixels in unit of rows. Accordingly, an element for vertical selection can be cut from a unit pixel.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a schematic configuration diagram showing a first embodiment of the present invention.

Fig. 2 is a potential diagram of unit pixel and vertical signal line in the first embodiment.

Fig. 3 is a timing chart at pixel selection in the first embodiment.

Figs. 4A to 4C show a potential diagram 1 of pixels of selection line in the first embodiment.

Figs. 5A to 5C show a potential diagram 2 of

pixels of selection line in the first embodiment.

Figs. 6A to 6E are cross-sectional structure diagrams showing a concrete configuration example of overflow path.

Fig. 7 is a schematic configuration diagram showing a variant of the first embodiment of the present invention.

Fig. 8 is a potential diagram of unit pixel and vertical signal line in of a variant of the first embodiment.

Fig. 9 is a timing chart at pixel selection in a variant of the first embodiment.

Fig. 10 is a schematic configuration diagram showing a second embodiment of the present invention.

Fig. 11 is a potential diagram of unit pixel and vertical signal line in the second embodiment.

Fig. 12 is a timing chart at pixel selection in the second embodiment.

Figs. 13A to 13D show a potential diagram 1 of pixels of selection line in the second embodiment.

Figs. 14A to 14C show a potential diagram 2 of pixels of selection line in the second embodiment.

Figs. 15A to 15D show a potential diagram 1 of pixels of non-selection line in the second embodiment.

Figs. 16A to 16C show a potential diagram 2 of pixels of non-selection line in the second embodiment

Fig. 17 is a schematic configuration diagram of an example of a camera system to which the present invention is applied.

Fig. 18 is a circuit diagram showing the configuration of a prior art unit pixel.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Hereinafter, embodiments of the present invention will be described with reference to the accompanying drawings.

Fig. 1 is a schematic configuration diagram of a CMOS image sensor according to a first embodiment of the present invention. In Fig. 1, unit pixels 10 are two-dimensionally arranged to constitute a pixel section; for simplicity, there are shown here only two pixels, unit pixel 10n,m in the n-th row, the m-th column and unit pixel 10n+1,m in the (n + 1)-th row, the m-th column. The structure of unit pixel 10 is the same for all pixels; hereinafter, as an example, the structure of unit pixel 10n,m in the n-th row, the m-th column will be described.

The unit pixel 10n,m comprises a photoelectric

transfer element, e.g., photodiode 11, transfer switch 12, floating diffusion (FD) 13 serving as a charge store part, reset switch 14, and amplifying transistor 15. As a photoelectric transfer element, photogate or embedded photodiode can be substituted for the photodiode 11.

In this example, N-channel enhancement type transistor, N-channel depression type transistor, and N-channel enhancement type transistor are used as the transfer switch 12, reset switch 14, and amplifying transistor 15, respectively. However, all or part of these transistors can also be replaced by P-channel transistors to constitute the circuit.

In the unit pixel 10n,m, the photodiode 11 is a p-n junction diode that photoelectrically converts incident light into signal charge of quantity in accordance with the quantity of the incident light and stores it. The transfer switch 12, connected between the photodiode 11 and floating diffusion 13, transfers the signal charge stored in the photodiode 11 to the floating diffusion 13. The floating diffusion 13 converts the transferred signal charge into a signal voltage and affords the voltage to the gate of the amplifying transistor 15.

The reset switch 14, connected between the floating diffusion 13 and vertical selection line 21, has a function to reset the potential of the floating diffusion 13 to that of pixel power source. The amplifying transistor 15, connected between power source line 22 and vertical signal line 23, amplifies the potential of the floating diffusion 13 and outputs the amplified potential to the vertical signal line 23. A pixel power source voltage is not limited to 3.3V, which is used as an example in this example.

Fig. 2 shows a potential distribution of unit pixel 10 and vertical signal line 23 in the first embodiment. In the figure, PD, TS, FD, RS, and AT designate photodiode 11, transfer switch 12, floating diffusion 13, reset switch 14, and amplifying transistor 15, respectively. For potentials of the floating diffusion 13 and amplifying transistor 15, a potential operation range at selection and a potential operation range at other times are shown by solid lines and dashed lines, respectively.

Vertical scanning circuit 24, provided to select unit pixels 10 in units of rows, is comprised of e.g., a shift register. From the vertical scanning circuit 24, vertical selection pulse ϕV (…, ϕVn, $\phi Vn+1$, …),

transfer pulse ϕT (···, ϕTn, ϕTn+1, ···), and reset pulse ϕR (···, ϕRn, ϕRn+1, ···) are output.

The vertical selection pulse ϕV (···, ϕVn, ϕVn+1, ···) is applied to the drain of reset switch 14 through the vertical selection line 21, the transfer pulse ϕT (···, ϕTn, ϕTn+1, ···) to the gate of transfer switch 12 through the transfer line 25, and the reset pulse ϕR (···, ϕRn, ϕRn+1, ···) to the gate of reset switch 14 through the reset line 26.

To the end of vertical signal line 23, vertical signal line output circuit 27 is connected for each column. As the vertical signal line output circuit 27, an output circuit of e.g., voltage mode type is used. Horizontal selection pulse ϕH (···, ϕHm, ···) from horizontal scanning circuit 28 is fed to the vertical signal line output circuit 27. The horizontal scanning circuit 28, provided to select unit pixels 10 in units of columns, is comprised of e.g., a shift register.

The output end of vertical signal line output circuit 27 is connected to horizontal signal line 29. To the horizontal signal line 29, one line of signals read into the vertical signal line output circuit 27 through the vertical signal line 23 from unit pixel 10 is output sequentially from the vertical signal line

output circuit 27 by horizontal scanning of the horizontal scanning circuit 28. The input end of horizontal signal line output circuit 30 is connected to the end of horizontal signal line 29.

Next, the pixel operation in a CMOS image sensor according to the first embodiment of the above configuration will be described using an example of selecting pixels of n-th line (n-th row). Herein, the timing chart of Fig. 3 will be used with reference to the potential diagrams of Figs. 4 and 5.

A time period ($t < t1$) until time t1 is non-selection state. In the non-selection state, since vertical selection pulse ϕVn is in Low level (0 V) and reset switch (RS) 14 is in off state, the potential of floating diffusion (FD) 13 is 0 V.

At time t1, the vertical selection pulse ϕVn changes from Low to High (3.3V), and at the same time, in response to the occurrence of reset pulse ϕRn, the reset switch 14 goes on and the potential of floating diffusion 13 of the n-th line is reset from 0 V to 3.3V. As a result, since the amplifying transistor (AT) 15 is turned on, pixels of the n-th line go into selection state ($t1 < t < t2$).

Upon the extinction of the reset pulse ϕRn at

time t2, the reset floating diffusion 13 is read. Consequently, an offset level (hereinafter, called a noise level) different for each different pixel is read into the vertical signal line 23 by the amplifying transistor 15 and output to the vertical signal line output circuit 27 (t2 < t <t3). The read-out noise level is held (sample held) within the vertical signal line output circuit 27.

Upon the occurrence of transfer pulse ϕTn at time t3, the transfer switch (TS) 12, because a potential below the gate thereof is deepened by the transfer pulse ϕTn applied to the gate, transfers signal charge stored in the photodiode (PD) 11 to the floating diffusion 13 (t3 < t < t4). The transfer of signal charge causes the potential of the floating diffusion 13 to change in accordance with the quantity of charge.

Upon the extinction of the transfer pulse ϕTn at time t4, a potential in accordance with the signal charge of the floating diffusion 13 is read into the vertical signal line 23 by the amplifying transistor 15 and output to the vertical signal line output circuit 27 (t4 < t < t5). The read-out signal level is held (sample held) within the vertical signal line output

circuit 27.

Upon entry to a horizontal valid period, signals read from pixels 10 into the vertical signal line output circuit 27 for each column are sequentially output to the horizontal signal line output circuit 30 through the horizontal signal line 29. At this time, in these output circuits 27 and 30, by subtracting a noise level from the signal level of unit pixel 10, a fixed pattern noise due to the dispersion of characteristics of unit pixel 10 is suppressed and a fixed pattern noise due to the dispersion of characteristics of the vertical signal line output circuit 27 is suppressed.

At time t6, the vertical selection pulse ϕVn changes from High to Low, and thereby pixels on the n-th line go into non-selection state, and at the same time, pixels on the next (n + 1)-th line go into selection state, and the above operation is repeated on the (n + 1)-th line.

Herein, a description will be made of pixels on non-selection lines. By driving the vertical selection pulse ϕV Low (0 V), pixel 10 can be put in non-selection state. This is because since a depression type transistor is used as the reset switch 14, when

the vertical selection pulse ϕV is 0 V, the floating diffusion 13 is always 0 V, and thereby the amplifying transistor 15 is always in cut-off state.

As described above, unit pixel 10 is comprised of photodiode 11, transfer switch 12, floating diffusion 13, reset switch 14, and amplifying transistor 15, and the potential of floating diffusion 13 is controlled through the reset switch 14, whereby one transistor can be cut because a vertical selection switch is not provided to provide the vertical selection function, as it would be in the case of conventional pixel structures.

When the vertical selection pulse ϕV is driven Low by incorporating a charge pump circuit, the gate of the transfer switch 12 can be put at a negative potential for a long period other than the period $t3 < t < t4$. In such a case, a dark current can be suppressed since holes can be implanted into the silicon interface of the transfer switch adjacent to the photodiode 11 for a long period of time. This produces a great effect, particularly when an embedded sensor structure is employed as the photodiode 11.

Although the foregoing description of operation, for simplicity, has been on all pixel independent

reading mode in which signals of pixels of all lines are independently read, the present invention is not limited to that mode. Of course, frame reading mode and field reading mode are also possible. In the former mode, signals of odd (even) lines are read in a first field and signals of even (odd) lines are read in a second field. In the latter mode, signals of two adjacent lines are read at the same time to add voltages, and combinations of two lines for the addition operation are changed on a field basis.

Herein, a description will be made of a concrete configuration of unit pixel 10. When signal charges are stored in the photodiode 11, as apparent from Fig. 4A, the floating diffusion 13 becomes 0 V. For this reason, during the charge storing, the surface potential of the transfer switch 12 must be 0 V or less. However, without a special process, there would be no path for discharging charges that overflow from the photodiode 11,

Accordingly, a pixel structure according to the present invention is made so that a diffusion layer connected to power source, e.g., the drain of the amplifying transistor 15 is laid out adjacently to the photodiode 11 and element separation between both is

made imperfect, whereby an overflow path is formed and excess charges are discharged (overflowed) via the path. By this process, an overflow path can be formed without increasing the dimension of unit pixel 10.

As concrete examples of forming an overflow path, various structures described below are possible. As shown in Figs. 6A to 6E, there are a structure (Fig. 6A) in which an overflow path is formed by reducing the width (distance) of an element separation region; a structure (Fig. 6B) in which an overflow path is formed by reducing the density of a P region for channel stop; and a structure (Fig. 6C) in which an overflow path is formed by positively forming an N^- region below a P region for channel stop.

In the case where an embedded sensor structure is used as the photodiode 11, there are a structure (Fig. 6D) in which an N^+(SR N^+) region for sensor is formed also in the pixel power source side to moderately form a lateral distance of an overflow path and further a high-density impurity is injected into the N^+ region of the pixel power source side to form a N^+ region for source/drain; and a structure (Fig. 6E) in which an N^- region is formed for an overflow path in the (Fig. 6D) structure.

A LOCOS (Local Oxidation of Silicon) oxide film shown in each of the structures of Figs. 6A to 6C is not necessarily necessary. However, in this case, to moderately form a lateral distance of an overflow path, as in the example of the (Fig. 6D) structure, it is desirable to implant ions to an N^+ region of photodiode 11 and an N^+ region of pixel power source adjacent to an overflow pulse with an identical mask.

As in each of the structures of Fig. 6A, and Figs. 6C to 6E, the silicon interface of overflow section is not depleted by forming the overflow path with a virtual gate. Accordingly, dark current occurs less frequently, compared with prior art overflow structures in which a transfer gate is used, in which case a silicon interface would be depleted. A greater effect is obtained particularly when an embedded sensor structure is used as the photodiode 11, because depleted portions of silicon interface can be completely eliminated.

Fig. 7 is a schematic configuration diagram of a variant of a first embodiment of the present invention. The first embodiment takes a configuration in which signals from pixels are output in voltage mode, while the variant takes a configuration in which signals from

pixels are output in current mode. Accordingly, the pixel structure of unit pixel is exactly the same as that of the first embodiment, except for the configuration of a signal output system.

A CMOS image sensor according to the variant takes a configuration in which horizontal selection switch 31 is connected between the end of vertical signal line 23 and horizontal signal line 29, and an operational amplifier 33 fed back by resistor 32 is placed at the end of horizontal signal line 29. That is, to output signals from pixels in current mode, the vertical signal line 23 and horizontal signal line 29 are fixed to a constant potential (Vbias) by the operational amplifier 33 fed back by the resistor 32 and the amplifying transistor 15 within unit pixel 10n,m is linearly operated by incorporating a power source circuit 34, for example, and reducing a source voltage to be afforded to pixels.

Although this variant is constructed in a way that incorporates the power source circuit 34 and reduces a source voltage to be afforded to pixels, the present invention is not limited to this construction. For example, by reducing a threshold voltage Vth of the amplifying transistor 15 within unit pixel 10n,m, the

amplifying transistor 15 can also be linearly operated.

Fig. 8 shows a potential distribution of unit pixel 10 and vertical signal line 23 in this variant. In Fig. 8, PD, TS, FD, RS, and AT designate photodiode 11, transfer switch 12, floating diffusion 13, reset switch 14, and amplifying transistor 15, respectively. For potentials of the floating diffusion 13 and amplifying transistor 15, a potential operation range at selection and a potential operation range at other times are shown by solid lines and dashed lines, respectively.

Fig. 9 is a timing chart for explaining the operation of a CMOS image sensor according to this variant. Fundamental portions of the operation of unit pixel 10n,m are the same as those of the first embodiment. Herein, to avoid an overlapping description, only different portions will be described.

Signals are read from pixels during a horizontal valid period. Noise levels are not read but only signal levels are read. Since a sample hold operation cannot be performed in a signal output system in the current mode as it could be in the voltage mode, fixed pattern noises of signal levels due to the characteristics of pixels are suppressed using a frame

memory in an external signal processing system.

Although Fig. 9 is a timing chart on the all pixel independent reading mode in which signals of pixels of all lines are independently read, the present invention is not limited to that mode. Of course, the frame reading mode and the field reading mode are also possible. In the former mode, signals of odd (even) lines are read in a first field and signals of even (odd) lines are read in a second field. In the latter mode, signals of two adjacent lines are read at the same time to add currents, and combinations of two lines for the addition operation are changed on a field basis.

Fig. 10 is a schematic configuration diagram of a CMOS image sensor according to a second embodiment of the present invention. In Fig. 10, unit pixels 40 are two-dimensionally arranged to constitute a pixel section; for simplicity, there are shown here only two pixels, unit pixel 40n,m in the n-th row, the m-th column and unit pixel 40n+1,m in the (n + 1)-th row, the m-th column. The structure of unit pixel 40 is the same for all pixels; hereinafter, as an example, the structure of unit pixel 40n,m in the n-th row, the m-th column will be described.

The unit pixel 40n,m comprises a photoelectric transfer element, e.g., photodiode 41, transfer switch 42, floating diffusion (FD) 43 serving as a charge store part, reset switch 44, amplifying transistor 45, and transfer selection switch 46. As a photoelectric transfer element, photogate or embedded photodiode can be substituted for the photodiode 41.

In this example, N-channel enhancement type transistor, N-channel depression type transistor, N-channel enhancement type transistor, and N-channel enhancement type transistor are used as transfer switch 42, reset switch 44, amplifying transistor 45, and transfer selection switch 45, respectively. However, all or part of these transistors can also be replaced by P-channel transistors to constitute the circuit.

In the unit pixel 40n,m, the photodiode 41 is a p-n junction diode of e.g., an embedded sensor structure that photoelectrically converts incident light into signal charge of quantity in accordance with the quantity of the incident light and stores it. The transfer switch 42, connected between the photodiode 41 and floating diffusion 43, transfers the signal charge stored in the photodiode 41 to the floating diffusion 43. The floating diffusion 43 converts the transferred

signal charge into a signal voltage and feeds the voltage to the gate of the amplifying transistor 45.

The reset switch 44, connected between the floating diffusion 43 and vertical selection line 51, has a function to reset the potential of the floating diffusion 43 to that of pixel power source. The amplifying transistor 45, connected between power source line 52 and vertical signal line 53, amplifies the potential of the floating diffusion 43 and outputs the amplified potential to the vertical signal line 53.

To the power source line 52, a voltage of e.g., 3.3 V is afforded from power source circuit 54. However, a source voltage is not limited to 3.3 V. Transfer selection switch 46, connected between transfer line 55 and transfer switch 42, performs transfer control for the transfer switch 42.

Fig. 11 shows a potential distribution of unit pixel 40 and vertical signal line 53 in the second embodiment. In Fig. 11, PD, TS, FD, RS, AT, and SS designate photodiode 41, transfer switch 42, floating diffusion 43, reset switch 44, amplifying transistor 45, and transfer selection switch 46, respectively. For potentials of the floating diffusion 43 and amplifying transistor 45, a potential operation range at selection

and a potential operation range at other times are shown by solid lines and dashed lines, respectively.

As apparent from Fig. 11, in this example, a photodiode of an embedded sensor structure is used as photodiode 41. That is, the photodiode is of such a sensor construction that P^+ hole store layer 47 is provided on the substrate surface of the p-n junction diode. For an overflow path of unit pixel 40, the pixel structures in Figs. 6A to 6E are employed, as in the first embodiment.

Vertical scanning circuit 56, provided to select unit pixels 40 in units of rows, is comprised of e.g., a shift register. From the vertical scanning circuit 56, vertical selection pulse ϕV (···, ϕVn, ϕVn+1, ···) is output. Vertical selection pulse ϕV (···, ϕVn, ϕVn+1, ···) is applied to the drain of reset switch 14 via the vertical selection line 51.

Vertical scanning circuit 57, provided to select unit pixels 40 in units of columns, is comprised of e.g., a shift register. From the horizontal scanning circuit 57, reset pulse ϕR (···, ϕRm, ···), transfer pulse ϕT (···, ϕTm, ···), and horizontal selection pulse ϕH (···, ϕHm, ···) are output. The transfer pulse ϕT (···, ϕTm, ···) is applied to the drain of transfer

selection switch 46 via the transfer line 55, and the reset pulse ϕR (···, ϕRm, ···) to the gate of reset switch 44 via the reset line 58.

Horizontal selection switch 60 is connected between the end of vertical signal line 53 and horizontal signal line 59. As the horizontal selection transistor 60, an N-channel transistor, for example, is used. Horizontal selection pulse ϕH (···, ϕHm, ···) output from horizontal scanning circuit 57 is fed to the gate of the horizontal selection transistor 60. An operational amplifier 62 fed back by resistor 61 is placed at the end of horizontal signal line 59.

A CMOS image sensor according to the second embodiment of the above configuration takes a configuration in which signals from pixels are output in the current mode. That is, the vertical signal line 53 and horizontal signal line 59 are fixed to a constant potential (Vbias) by the operational amplifier 62 fed back by the resistor 61 and the amplifying transistor 45 within unit pixel 40n,m is linearly operated by incorporating a power source circuit 54 and reducing a source voltage to be afforded to pixels.

Although this embodiment is configured so that the amplifying transistor 45 is linearly operated by

incorporating the power source circuit 54 and reducing a source voltage to be afforded to pixels, the present invention is not limited to this configuration. For example, by reducing a threshold voltage Vth of the amplifying transistor 45 within unit pixel 40n,m, the amplifying transistor 45 can be linearly operated.

Next, the pixel operation in a CMOS image sensor according to the second embodiment of the above configuration will be described using an example of selecting pixels of n-th line. Herein, the timing chart of Fig. 12 will be used with reference to the potential diagrams of Figs. 13 and 14.

A time period (t < t1) until time t1 is non-selection state. In the non-selection state, since vertical selection pulse ϕVn is in Low level (0 V) and reset switch (RS) 44 is in off state, the potential of floating diffusion (FD) 43 is 0 V.

At time t1, the vertical selection pulse ϕVn changes from Low to High (3.3V). The gate potential of the amplifying transistor (AT) 45 increases because a depression type transistor is used as the reset transistor 44 (t1 < t < t2).

At this time, the amplifying transistor 45 may comes on depending on the potential setting thereof or

the potential of the vertical signal line 53. This example assumes that the amplifying transistor 45 is cut off. At this point, however, since the horizontal selection switch 60 is off and no influence is exerted on the horizontal signal line 59, it does not matter in which state the amplifying transistor 45 is.

In response to the occurrence of reset pulse ϕ Rm at time t2, the reset switch 44 comes on and the potential of floating diffusion 43 in the n-th line, the m-th column is reset from 0 V to 3.3 V. Since this results in the amplifying transistor (AT) 45 turning on, unit pixel 40n,m in the n-th line, the m-th column goes into the selection state ($t2 < t < t3$).

Upon the extinction of the reset pulse ϕRm at time t3, the reset floating diffusion 43 is read. Consequently, an offset level (hereinafter, called a noise level) different for each pixel is read into the vertical signal line 53 ($t3 < t < t4$). The read-out noise level is, in response to the horizontal selection pulse ϕHm that occurred at time t2, output to the horizontal signal line 59 by the horizontal selection switch 60 that is on.

Upon the occurrence of transfer pulse ϕTm at time t4, the transfer switch (TS) 42, because a

potential below the gate thereof is deepened by the transfer pulse ϕTn applied to the gate, transfers signal charge stored in the photodiode (PD) 41 to the floating diffusion 43 (t4 < t < t5). The transfer of the signal charge causes the potential of the floating diffusion 43 to change in accordance with the quantity of charge.

Upon the extinction of the transfer pulse ϕTm at time t5, a potential in accordance with the signal charge of the floating diffusion 43 is read into the vertical signal line 53 by the amplifying transistor 45 (t5 < t < t6). The read-out noise level is output to the horizontal signal line 59 by the horizontal selection switch 60.

At time t7, the vertical selection pulse ϕVn changes from High to Low, whereby pixels on the n-th line go into non-selection state, and at the same time, pixels on the next (n + 1)-th line go into selection state, and the above operation is repeated on the (n + 1)-th line.

As described above, for one pixel, noise level and signal level are sequentially obtained in that order (a reverse order from signal level to noise level is also permissible). This operation is called a pixel

point sequential reset operation.

The pixel point sequential reset operation has the following advantages:

① Since noise output and signal output take an identical path including the horizontal selection switch 60, a fixed pattern noise due to dispersion between paths will not occur in principle.

② Since noise level and signal level are sequentially output, the difference between noise level and signal level can be obtained by a differential circuit such as a correlated duplex sampling circuit (CDS circuit) without using frame memory and line memory in an external signal processing system, so that the system can be simplified.

A series of pixel point sequential reset operations described above must be performed at a high speed. For this reason, signals from pixels are output in the current mode that is advantageous in terms of operation speed. However, without being limited to a mode of current mode output, if speed requirements are satisfied, a mode of voltage mode output can also be taken, as in a CMOS image sensor according to the first embodiment.

As apparent from the potential diagrams of Figs.

15 and 16, the operation of pixels not selected does not matter particularly even if transfer pulse ϕTm and reset pulse ϕRm are shared in column direction.

Although the foregoing description of operation, for simplicity, is on the all pixel independent reading mode in which signals of pixels of all lines are independently read, the present invention is not limited to that mode. Of course, frame reading mode and field reading mode are also possible. In the former mode, signals of odd (even) lines are read in a first field and signals of even (odd) lines are read in a second field. In the latter mode, signals of two adjacent lines are read at the same time to add currents, and combinations of two lines for the addition operation are changed on a field basis.

In the CMOS image sensor according to the above second embodiment, adjacent ϕTm-1 and reset pulse ϕRm can be also be shared, and thereby the wiring can be cut.

By positively providing capacity to a node connected to the gate of transfer selection switch 46 and the gate of transfer switch 42, when vertical selection pulse ϕVn changes from High to Low when t > t7, the gate potential of the transfer switch 42 can be

made negative. By this arrangement, since holes can be implanted into the silicon interface of transfer switch 42 adjacent to the photodiode 41, a dark current can be suppressed.

Furthermore, the power source circuit 54 can be cut by shifting (in this example, e.g., 1.5 V shift) the potential (Vbias) of vertical signal line 53, the potential of amplifying transistor 45, and the entire source voltage.

A variant of the second embodiment can be constructed so that current output is performed by transferring the role of the amplifying transistor 45 as source follower resistance load to the horizontal selection switch 60. That is, a current output operation is performed as described below.

Assume that the horizontal selection switch 60 operates in a linear area. The potential of horizontal signal line 59 is held constant, for example, by using an operational amplifier 33 fed back by a resistor. By doing so, a source follower loaded with a resistor is formed by the amplifying transistor 46 and the horizontal selection switch 60, a current flows through the horizontal signal line 59 in accordance with the potential of floating diffusion 43, and a voltage in

accordance with the potential of floating diffusion 43 develops at the output end of the operational amplifier.

Fig. 17 is a schematic configuration diagram of an example of a camera system to which the present invention is applied. In Fig. 17, incident light (image light) from an object (not shown) forms an image on the imaging surface of imaging element 72 by an optical system including lens 71 and other elements. As the imaging element 72, a CMOS image sensor according to the foregoing first embodiment or variant thereof, or the second embodiment is used.

The imaging element 72 is driven based on a variety of timings output from driving circuit 73 including a timing generator and the like. An imaging signal output from the imaging element 72 is subjected to various signal operations in signal processing circuit 74 before being output as an image signal.

As described above, according to the present invention, unit pixels arranged in a matrix form are comprised of a photoelectric transfer element, a transfer switch, a charge store part, a reset switch, and an amplifying element, and pixels are selected in units of rows by controlling a reset potential afforded to the reset switch, whereby an element for vertical

selection can be cut, making reduction of pixel size possible.

What Is Claimed Is:

1. A solid-state imaging element, comprising:

unit pixels, arranged in a matrix form, which have photoelectric transfer elements, transfer switches for transferring charges stored in said photoelectric transfer elements, charge store parts for storing charges transferred by said transfer switches, reset switches for resetting said charge store parts, and amplifying elements for outputting signals in accordance with the potential of said charge store parts to vertical signal lines;

a vertical scanning circuit for selecting pixels in units of rows by controlling a reset potential afforded to said reset switches;

a horizontal scanning circuit for sequentially selecting signals output to said vertical signal lines in units of columns; and

an output circuit for outputting signals selected by said horizontal scanning circuit via horizontal signal lines.

2. A solid-state imaging element as claimed in claim 1, wherein said vertical scanning circuit affords vertical selection pulses sequentially output during vertical scanning to said reset switches as a reset

potential thereof.

3. A solid-state imaging element as claimed in claim 1, wherein said charge store part is floating diffusion.

4. A solid-state imaging element as claimed in claim 1, wherein said reset switches comprise a depression type transistor.

5. A solid-state imaging element as claimed in claim 1, wherein said output circuit outputs signals read into said vertical signal lines in voltage mode.

6. A solid-state imaging element as claimed in claim 1, wherein said output circuit outputs signals read into said vertical signal lines in current mode.

7. A solid-state imaging element as claimed in claim 1, wherein said unit pixels include an overflow path between said photoelectric transfer element and an area to which a pixel source voltage is afforded, said overflow path being used to discharge excess charges of said photoelectric transfer element.

8. A solid-state imaging element as claimed in claim 1, wherein a negative potential is applied to the control electrode of said transfer switches.

9. A solid-state imaging element as claimed in claim 1, wherein said unit pixels include a transfer

selection switch for selecting a transfer operation of said transfer switches.

10. A solid-state imaging element as claimed in claim 9, wherein said transfer selection switch makes a controlled input of said vertical selection pulses.

11. A solid-state imaging element as claimed in claim 9, wherein said output circuit outputs signals read into said vertical signal lines in current mode.

12. A method for driving a solid-state imaging element including unit pixels, arranged in a matrix form, which have photoelectric transfer elements, transfer switches for transferring charges stored in said photoelectric transfer elements, charge store parts for storing charges transferred by said transfer switches, reset switches for resetting said charge store parts, and amplifying elements for outputting signals in accordance with the potential of said charge store parts to vertical signal lines, said method comprising the step of:

selecting pixels in units of rows by controlling a reset potential afforded to said reset switches.

13. A method for driving a solid-state imaging element as claimed in claim 12, further comprising the step of:

outputting signals read into said vertical signal lines in voltage mode.

14. A method for driving a solid-state imaging element as claimed in claim 12, further comprising the step of:

outputting signals read into said vertical signal lines in current mode.

15. A camera system using a solid-state imaging element as an imaging device, said solid-state imaging element, comprising:

unit pixels, arranged in a matrix form, which have photoelectric transfer elements, transfer switches for transferring charges stored in said photoelectric transfer elements, charge store parts for storing charges transferred by said transfer switches, reset switches for resetting said charge store parts, and amplifying elements for outputting signals in accordance with the potential of said charge store parts to vertical signal lines;

a vertical scanning circuit for selecting pixels in units of rows by controlling a reset potential afforded to said reset switch;

a horizontal scanning circuit for sequentially selecting signals output to said vertical signal lines

in units of columns; and

an output circuit for outputting signals selected by said horizontal scanning circuit via horizontal signal lines.

ABSTRACT

Since the great number of elements constituting a unit pixel having an amplification function would hinder reduction of pixel size, unit pixel n,m arranged in a matrix form is comprised of a photodiode, a transfer switch for transferring charges stored in the photodiode, a floating diffusion for storing charges transferred by the transfer switch, a reset switch for resetting the floating diffusion, and an amplifying transistor for outputting a signal in accordance with the potential of the floating diffusion to a vertical signal line, and by affording vertical selection pulse ϕVn to the drain of the reset switch to control a reset potential thereof, pixels are selected in units of rows.

FIG. 1

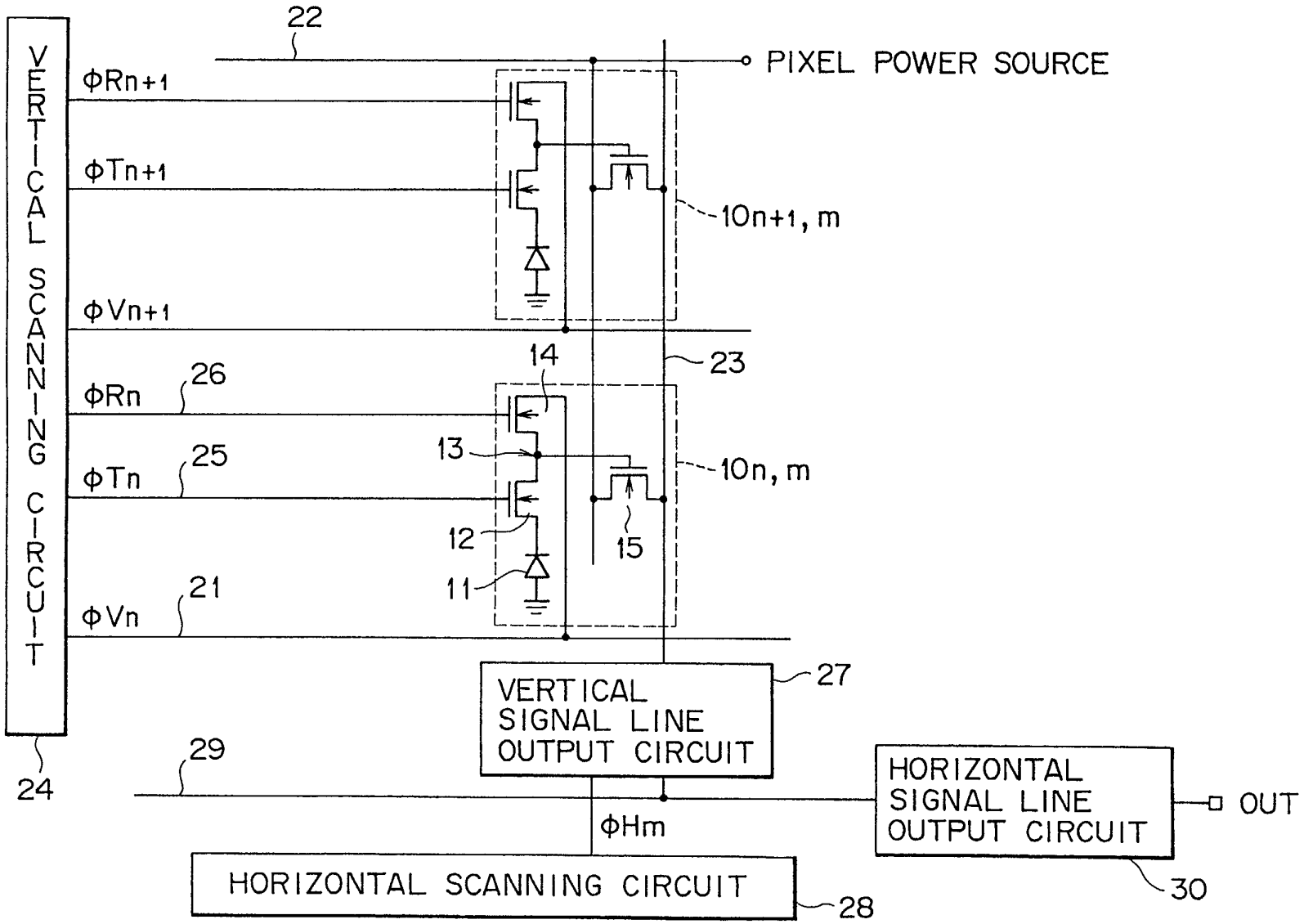


FIG. 2

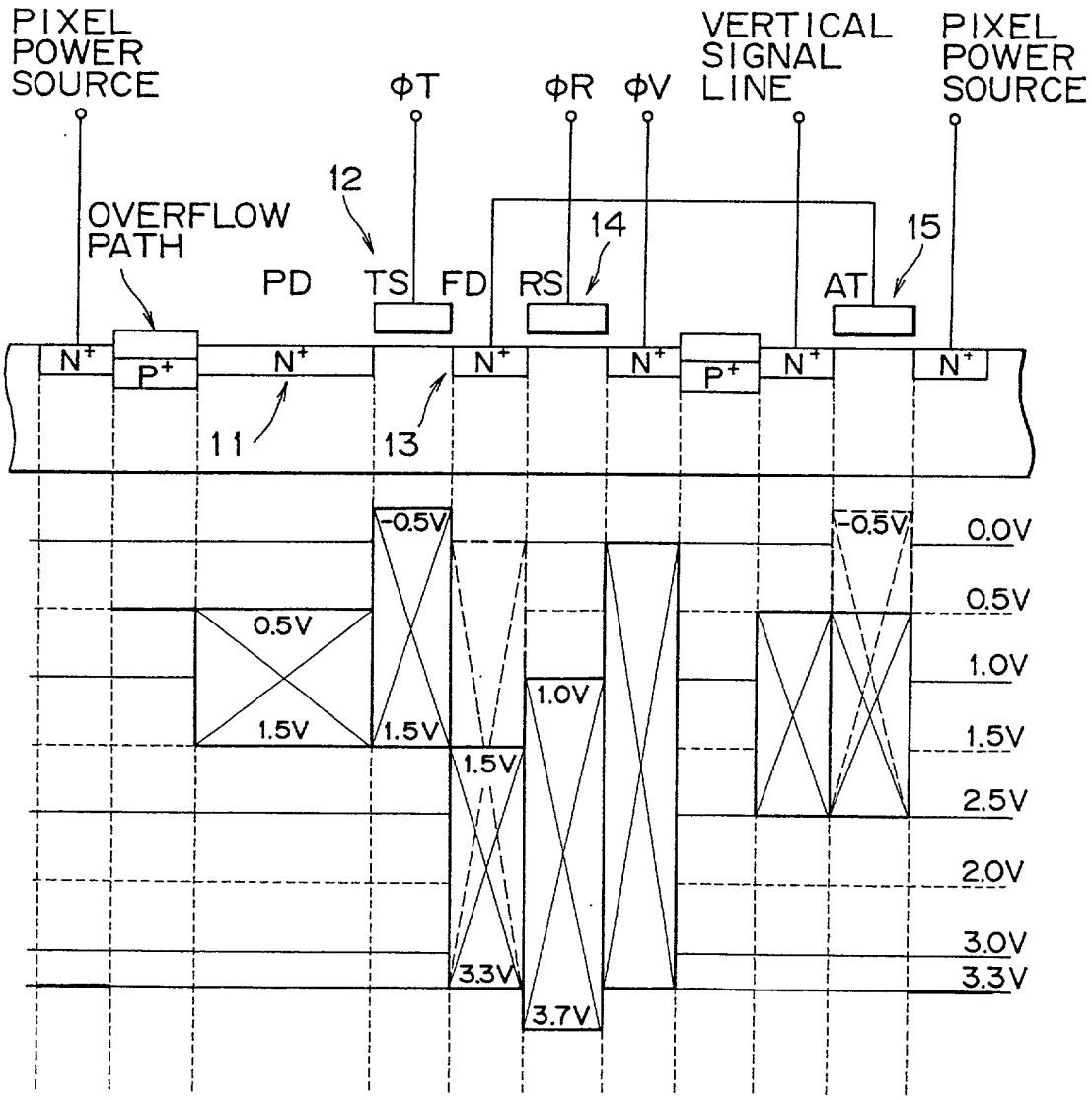

PIXEL POWER SOURCE
OVERFLOW PATH
12
φT
φR
φV
VERTICAL SIGNAL LINE
PIXEL POWER SOURCE
14
15
PD
TS
FD
RS
AT
N+
P+
N+
N+
N+
P+
N+
N+
11
13
-0.5V
-0.5V
0.5V
1.5V
1.5V
1.5V
1.0V
3.3V
3.7V
0.0V
0.5V
1.0V
1.5V
2.5V
2.0V
3.0V
3.3V

FIG. 3

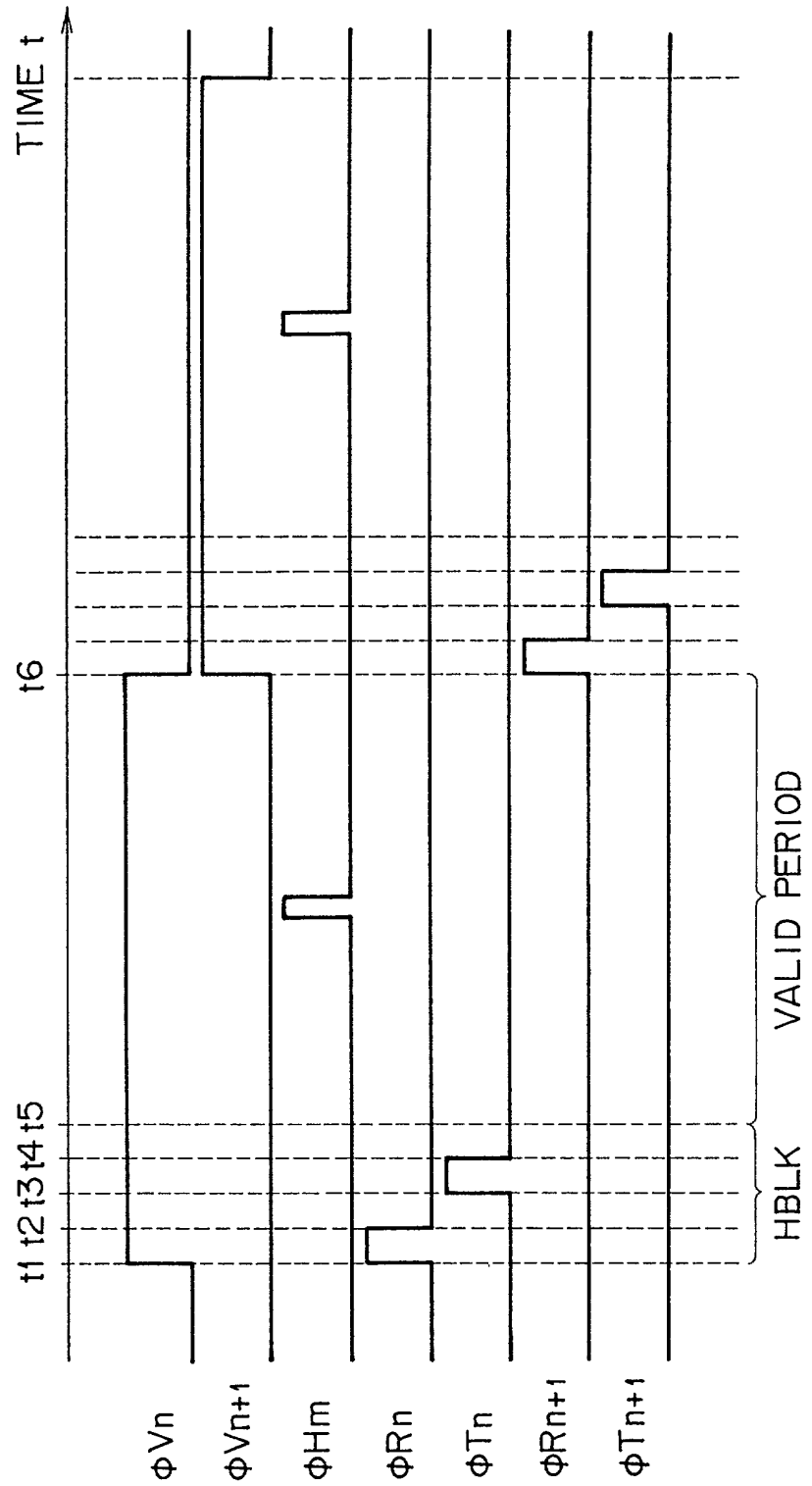

TIME t
t1 t2 t3 t4 t5
t6
HBLK
VALID PERIOD
φVn
φVn+1
φHm
φRn
φTn
φRn+1
φTn+1

FIG. 4A t<t1 NON-SELECTION STATE

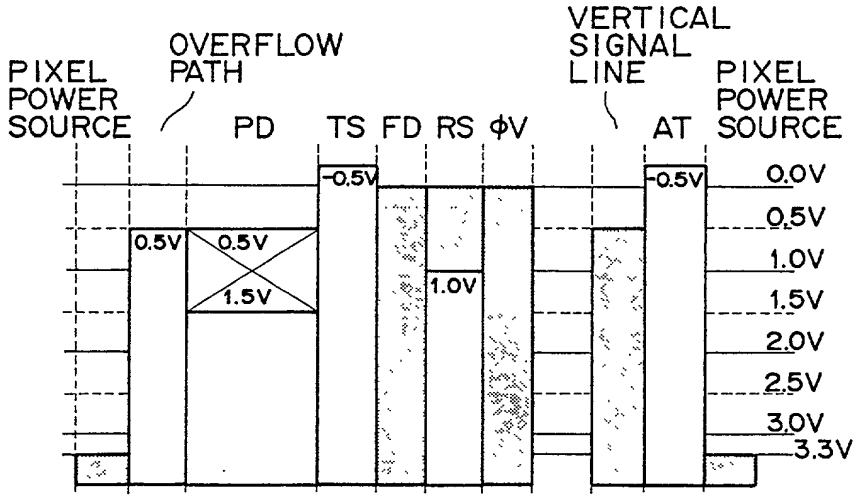


FIG. 4B t1<t<t2 FD RESET

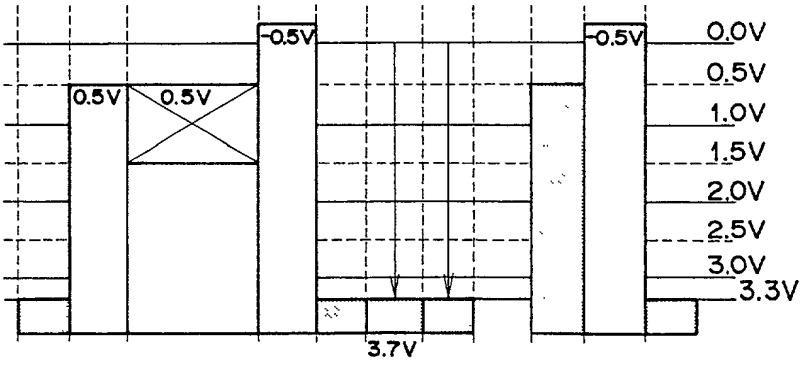


FIG. 4C t2<t<t3 OFFSET LEVEL (NOISE LEVEL) READ-OUT

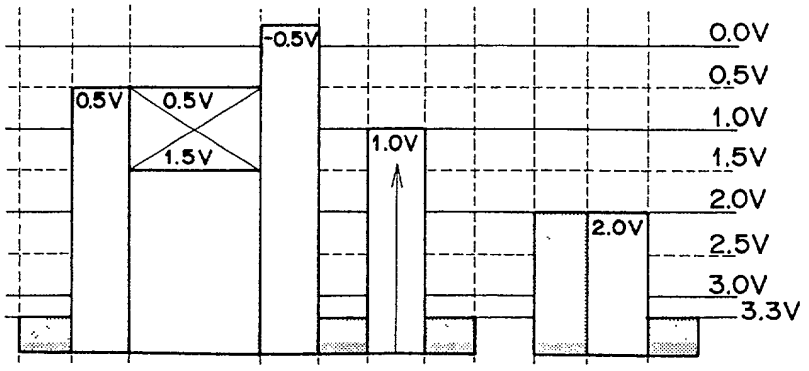


FIG. 5A t3<t<t4 TRANSFER OF SIGNAL CHARGE FROM PD TO FD

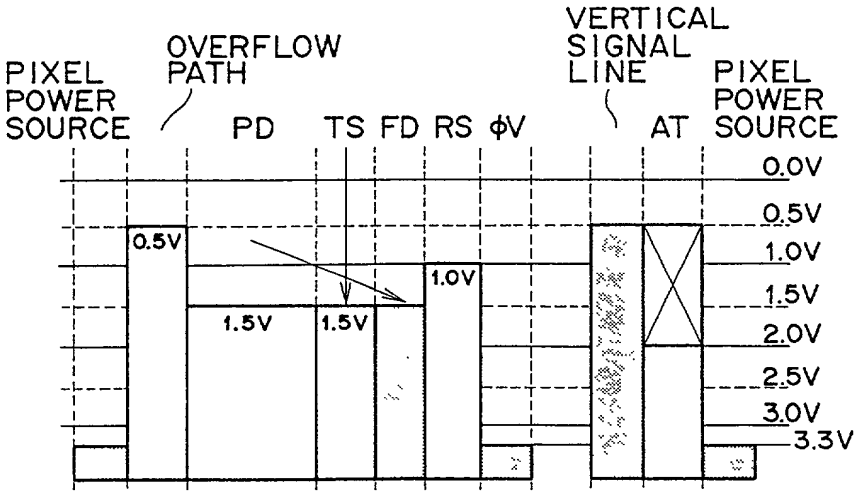


FIG. 5B t4<t<t5 SIGNAL LEVEL READ-OUT

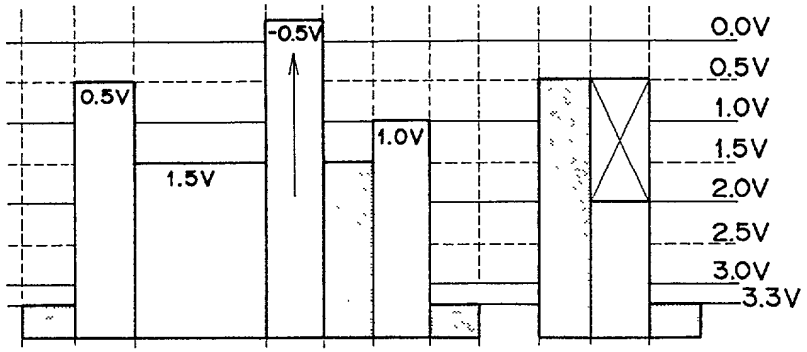


FIG. 5C t6<t NON-SELECTION STATE

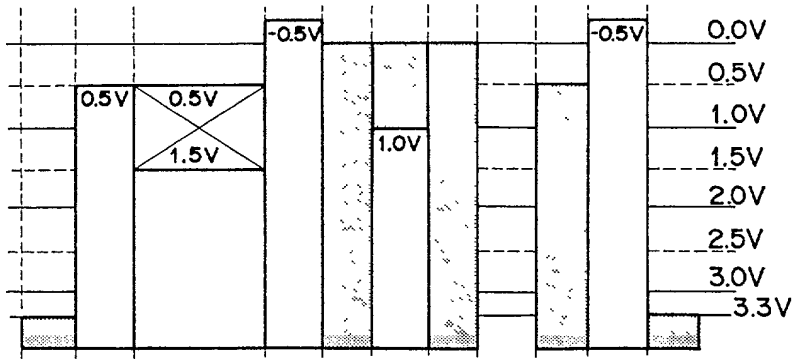
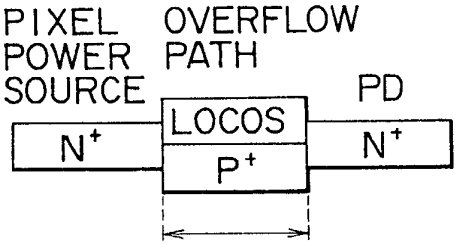
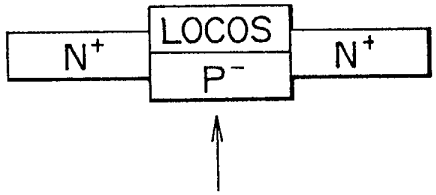


FIG. 6A



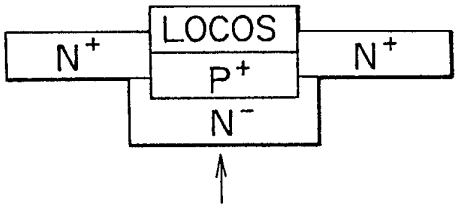
THE DISTANCE IS REDUCED

FIG. 6B



THE DENSITY OF P REGION OF CHANNEL STOP IS REDUCED

FIG. 6C



N⁻ REGION IS POSITIVELY FORMED

FIG. 6D

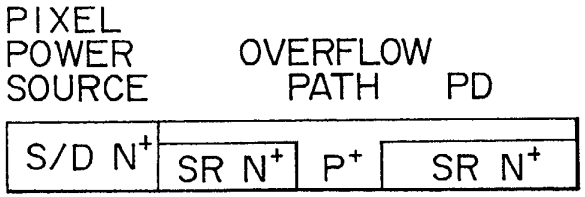


FIG. 6E

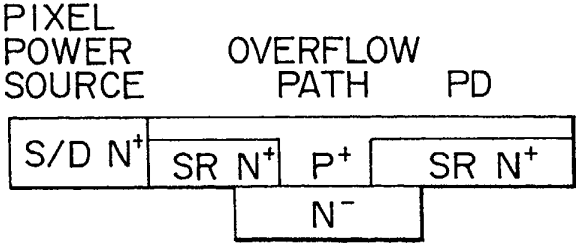


FIG. 7

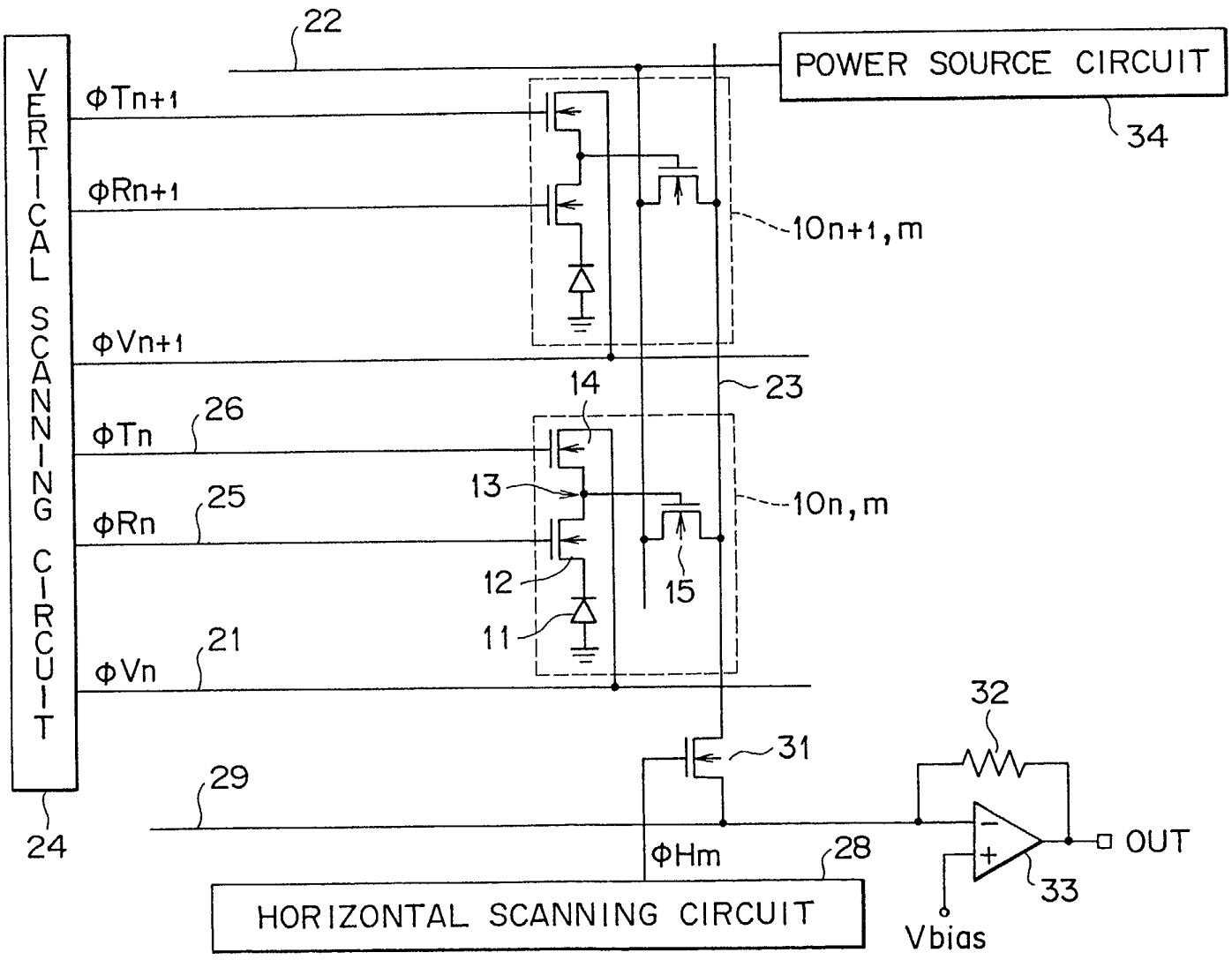


FIG. 8

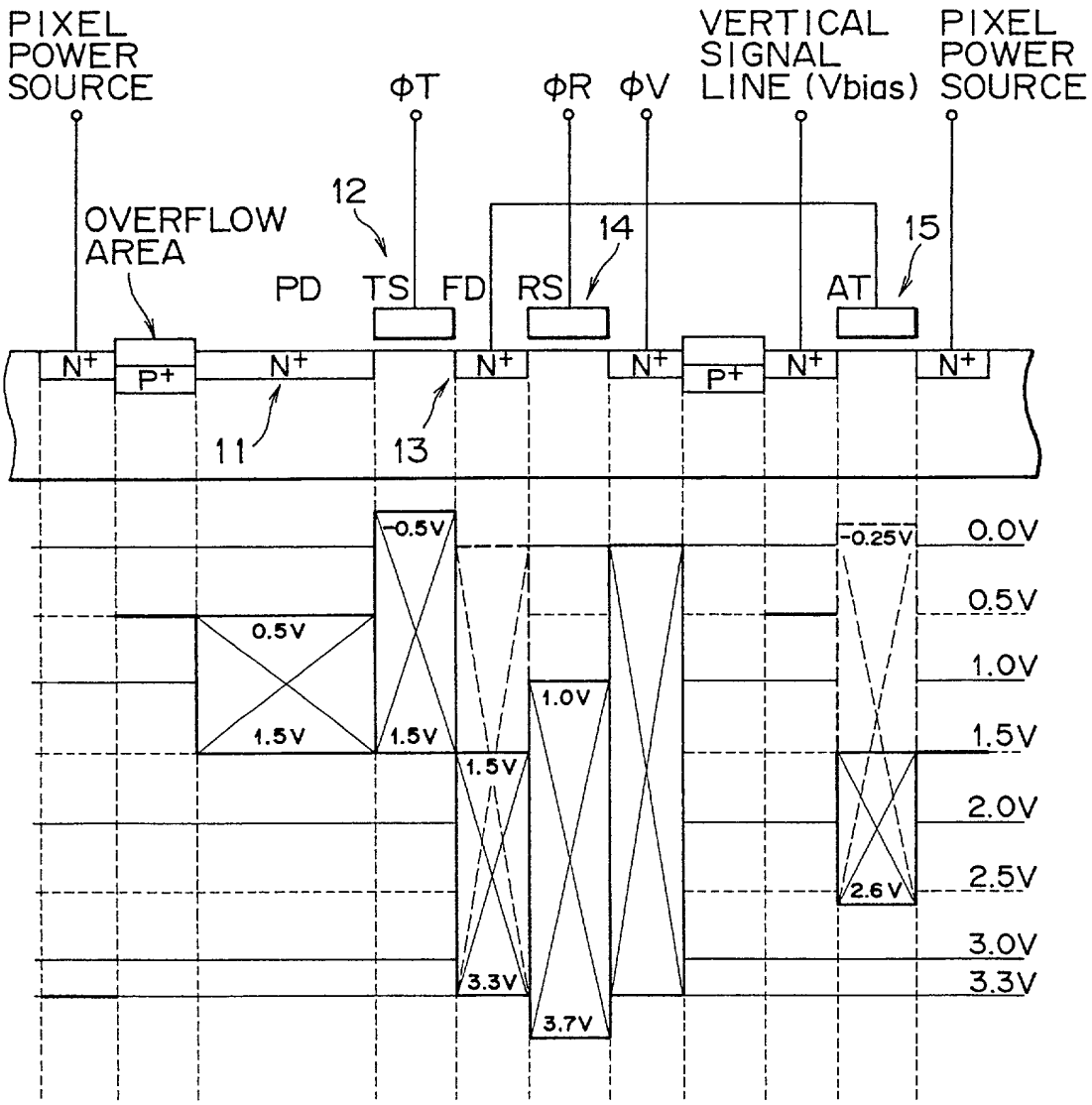

PIXEL POWER SOURCE
ΦT
ΦR
ΦV
VERTICAL SIGNAL LINE (Vbias)
PIXEL POWER SOURCE
OVERFLOW AREA
12
14
15
PD
TS
FD
RS
AT
N+
P+
11
13
-0.5V
-0.25V
0.0V
0.5V
1.0V
1.5V
2.0V
2.5V
3.0V
3.3V
2.6V
3.7V

FIG. 9

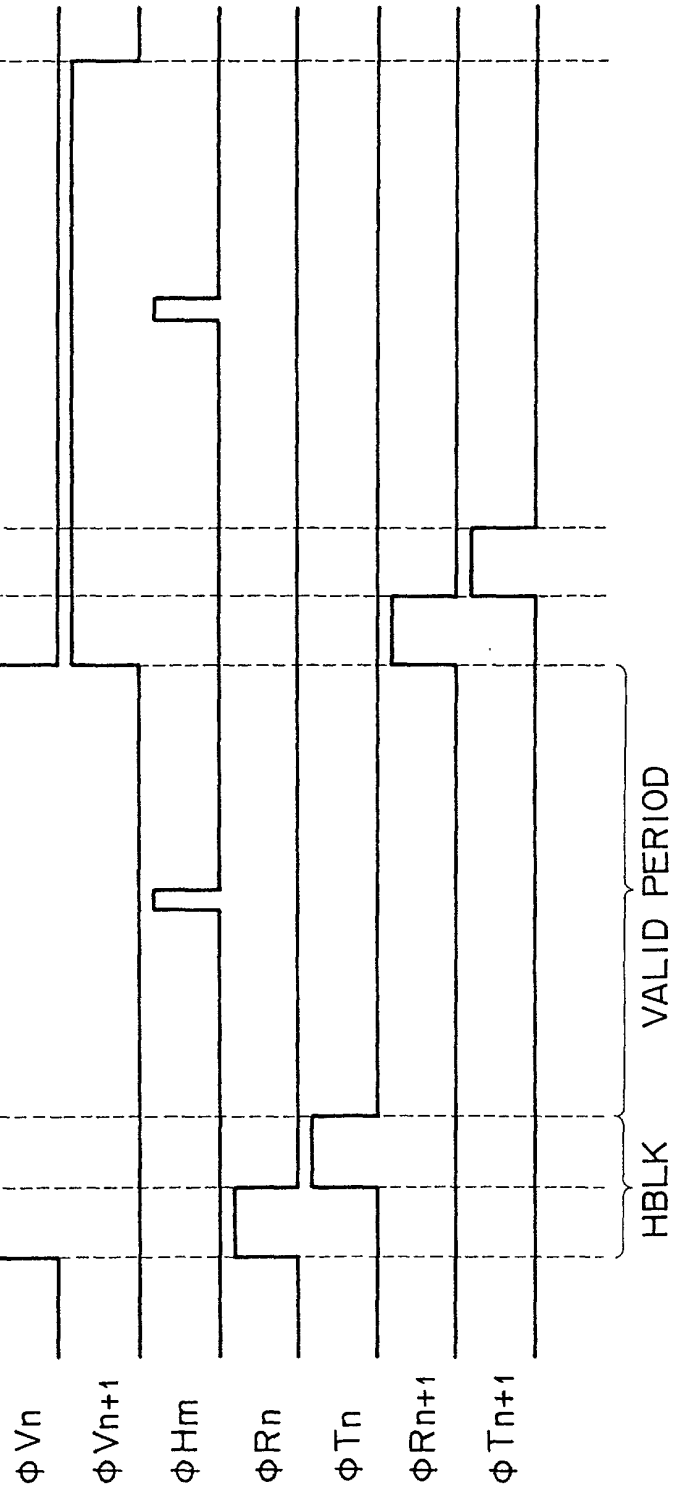


FIG. 10

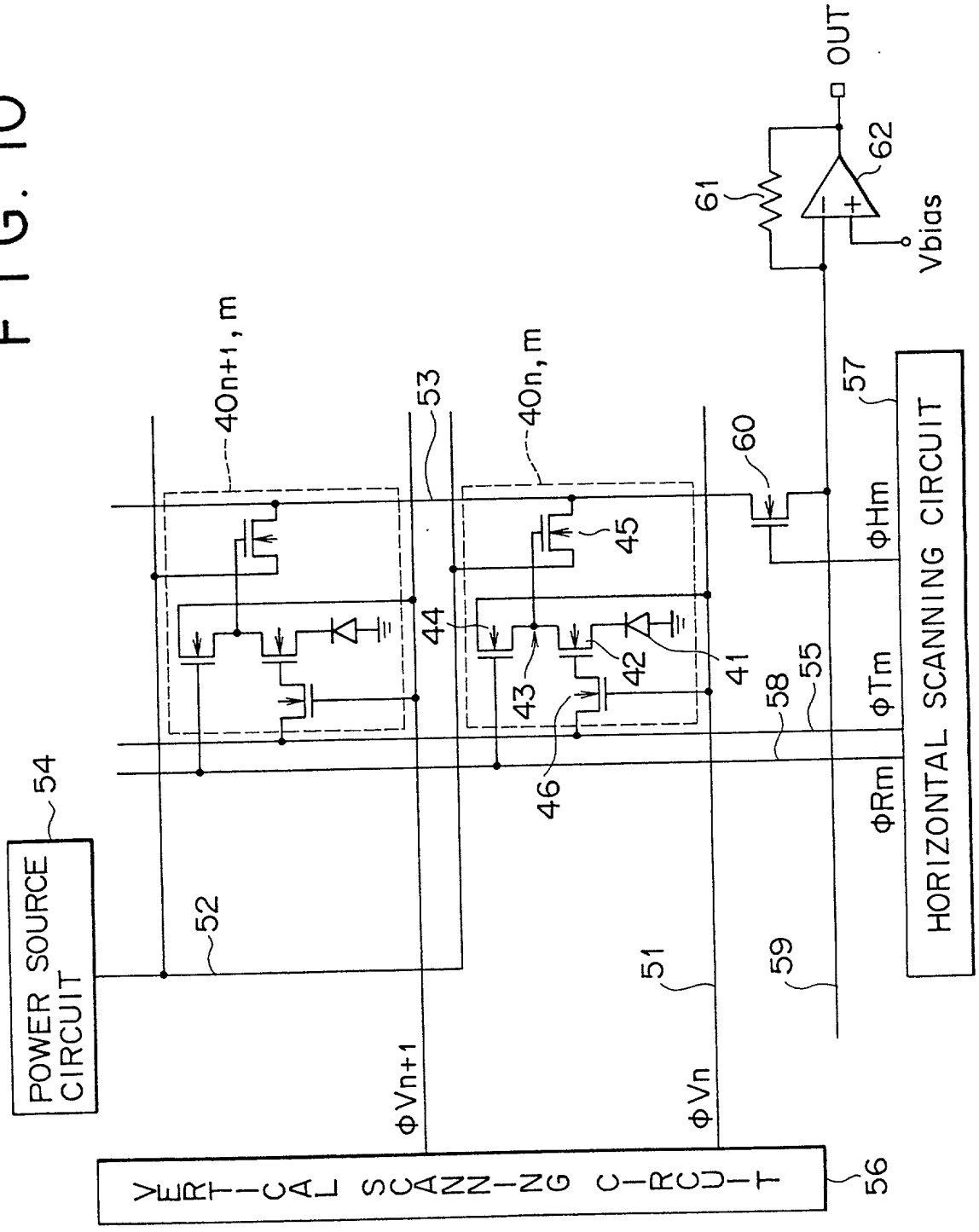

POWER SOURCE CIRCUIT
54
52
40n+1, m
53
40n, m
60
57
61
OUT
62
Vbias
45
44
43
42
41
46
58
55
φHm
φTm
φRm
HORIZONTAL SCANNING CIRCUIT
φVn+1
φVn
51
59
VERTICAL SCANNING CIRCUIT
56

FIG. 11

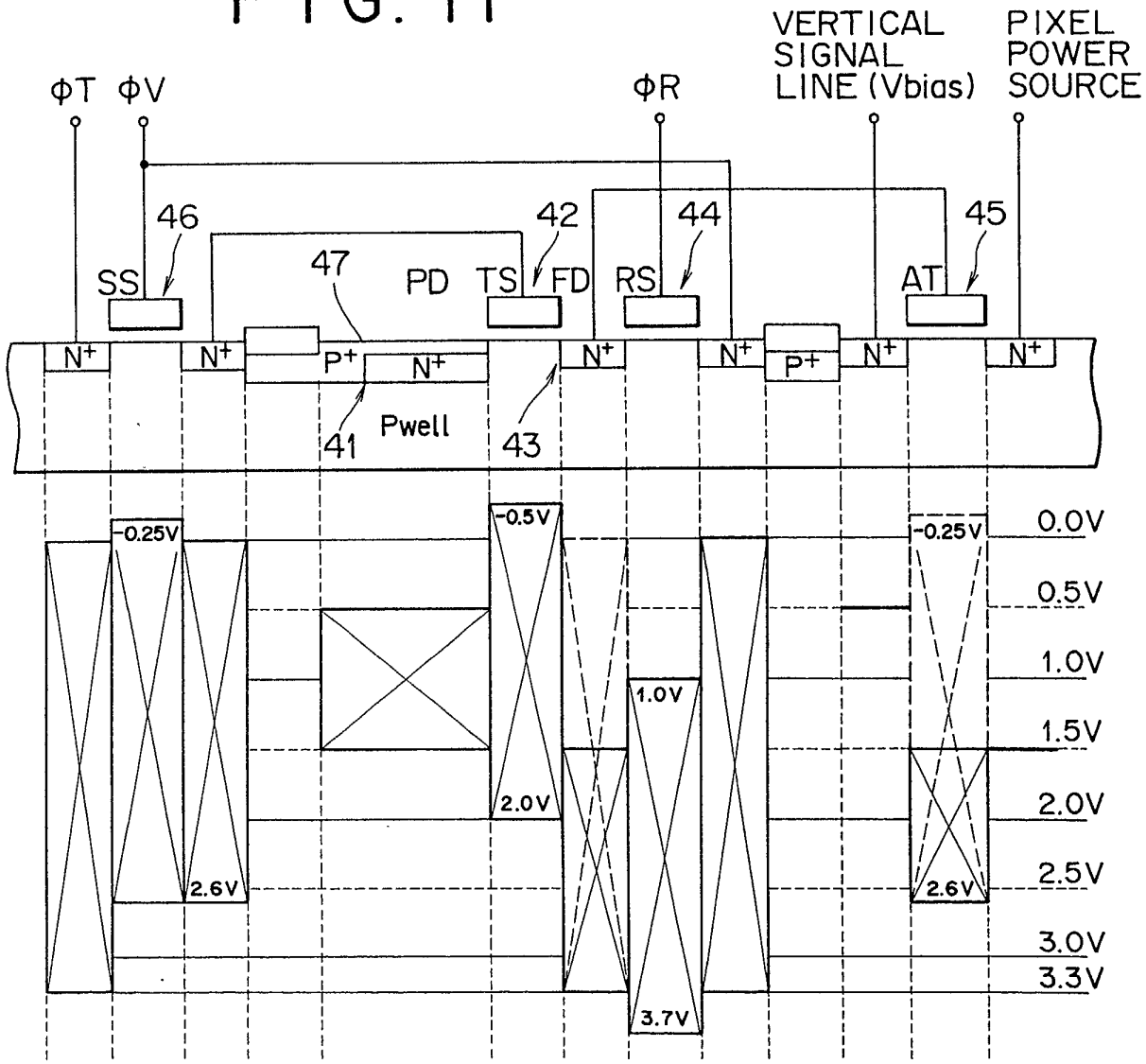

ΦT
ΦV
ΦR
VERTICAL SIGNAL LINE (Vbias)
PIXEL POWER SOURCE
46
42
44
45
47
SS
PD
TS
FD
RS
AT
N+
N+
P+
N+
N+
N+
N+
P+
N+
N+
41
Pwell
43
-0.25V
-0.5V
-0.25V
2.6V
2.0V
1.0V
2.6V
3.7V
0.0V
0.5V
1.0V
1.5V
2.0V
2.5V
3.0V
3.3V

FIG. 12

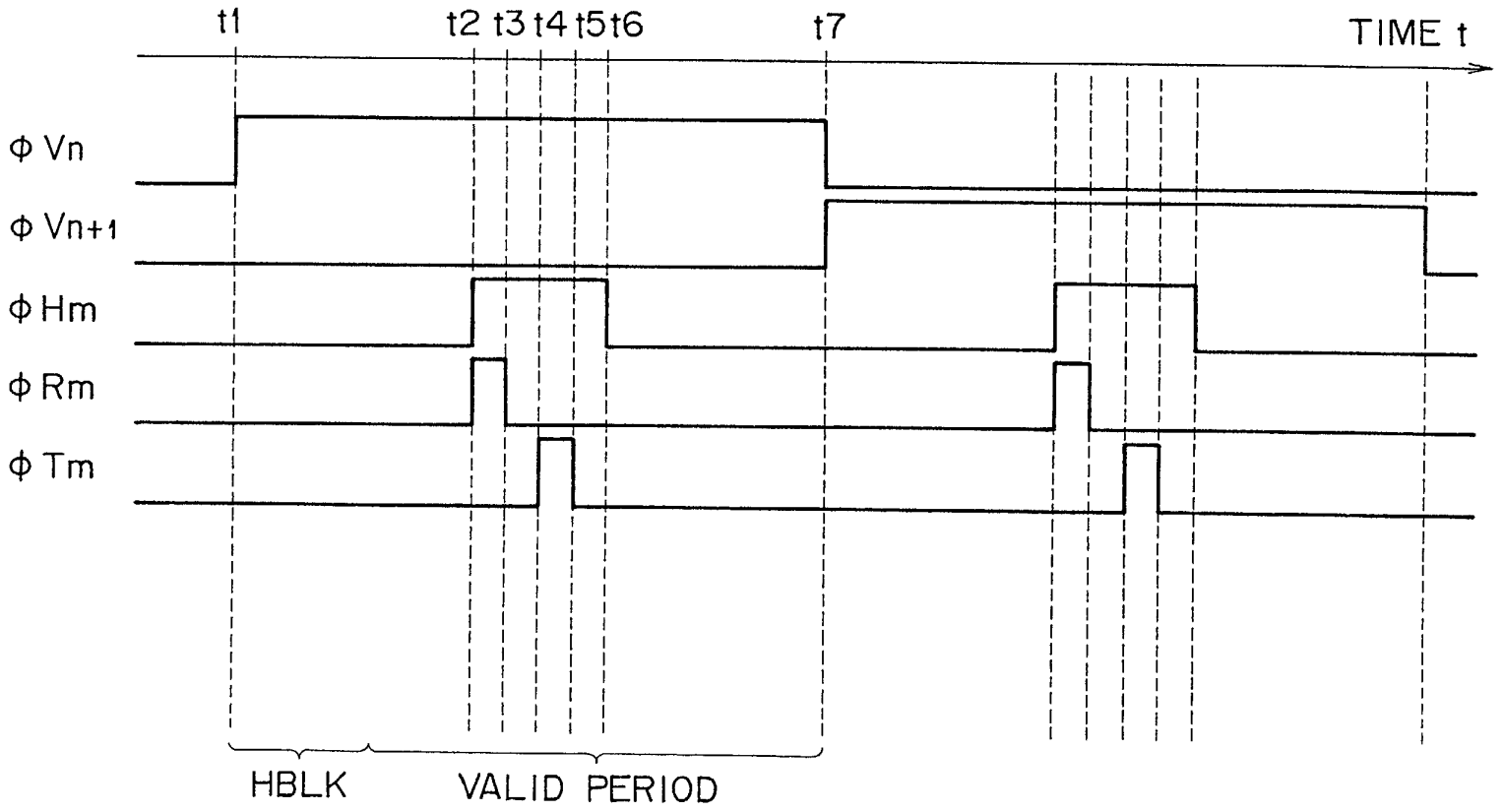


FIG. 13A t<t1 NON-SELECTION STATE

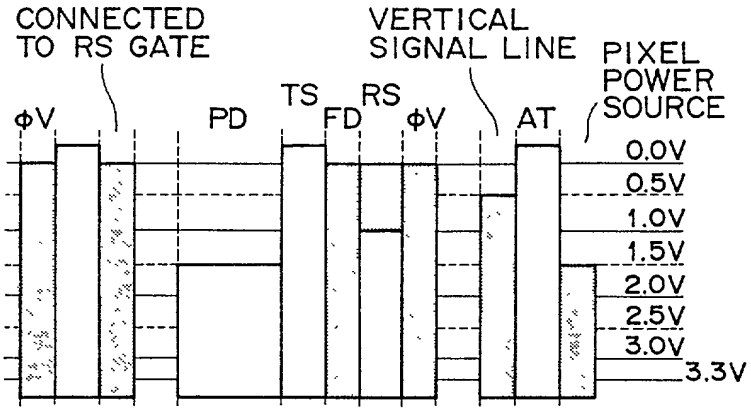


FIG. 13B t1<t<t2 SELECTION

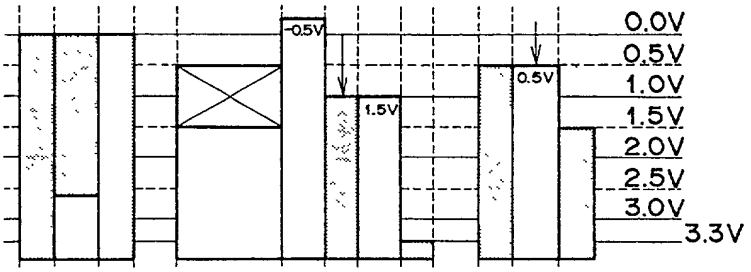


FIG. 13C t2<t<t3 FD RESET

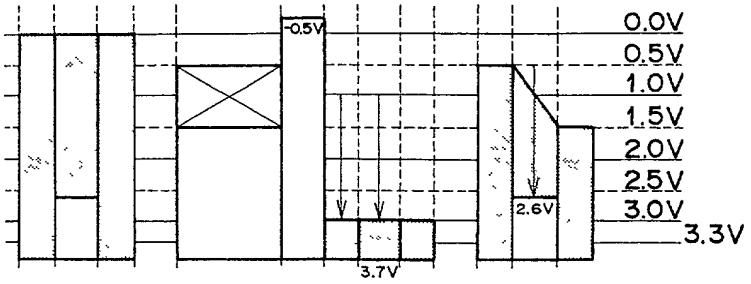


FIG. 13D t3<t<t4 FD RESET

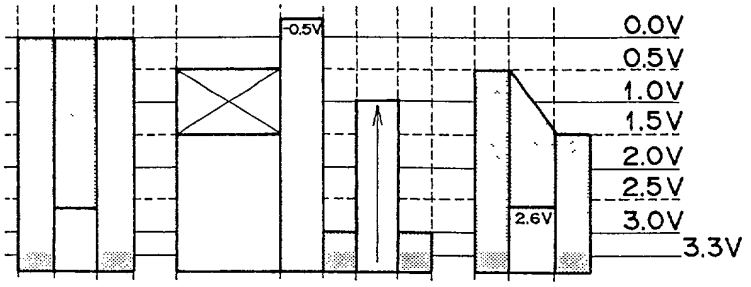


FIG. 14A t4<t<t5 TRANSFER OF STORED CHARGES FROM PD TO FD

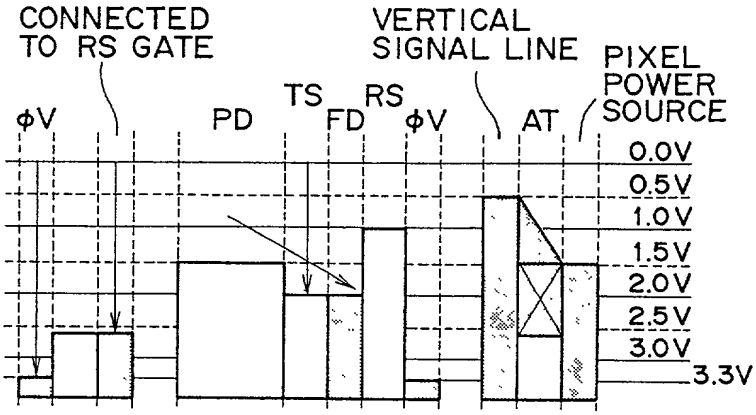


FIG. 14B t5<t<t6 SIGNAL LEVEL READ-OUT

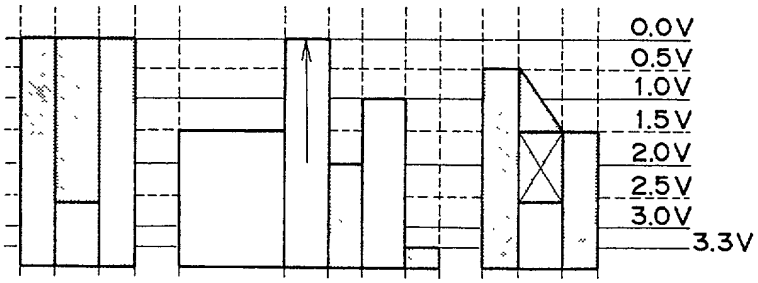


FIG. 14C t7<t NON-SELECTION

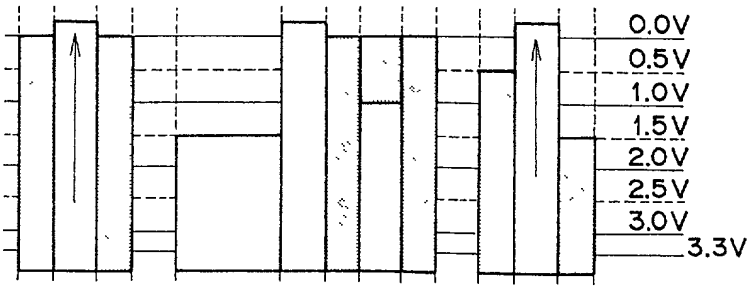


FIG. 15A t<t1

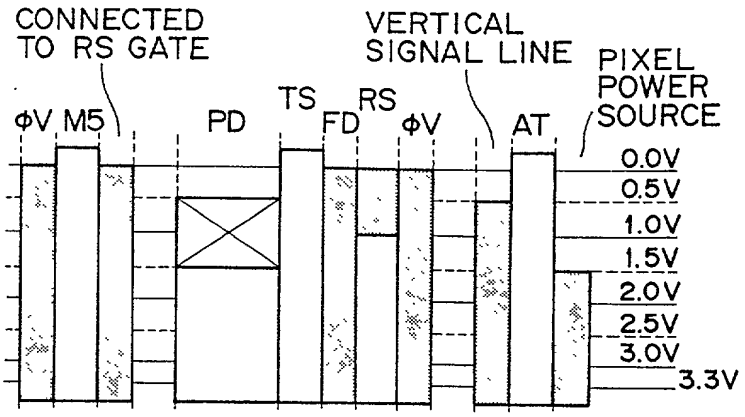


FIG. 15B t1<t<t2

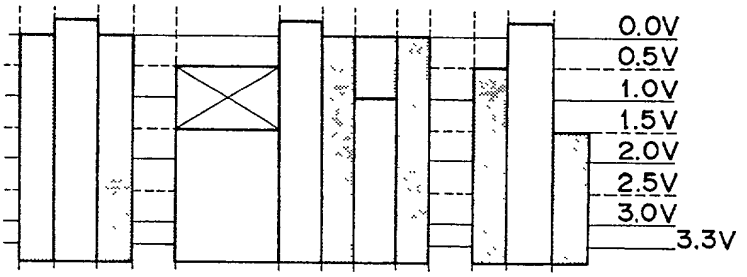


FIG. 15C t2<t<t3

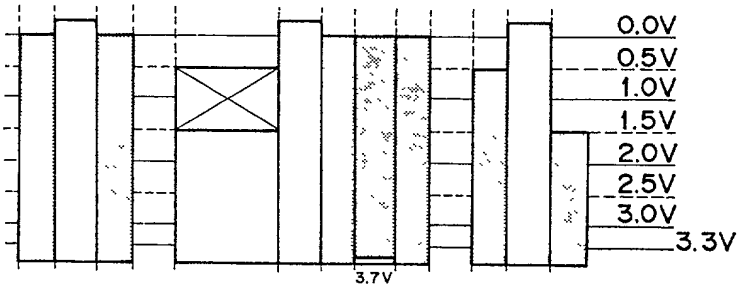


FIG. 15D t3<t<t4

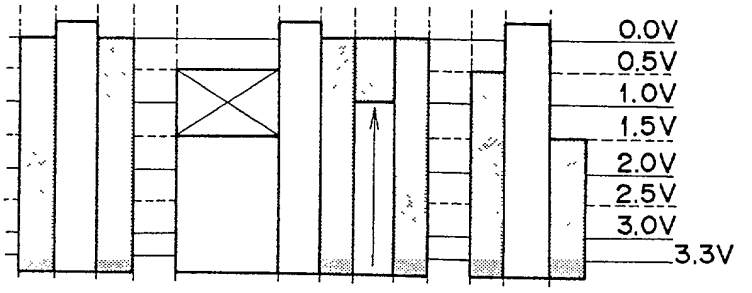


FIG. 16A t4<t<t5

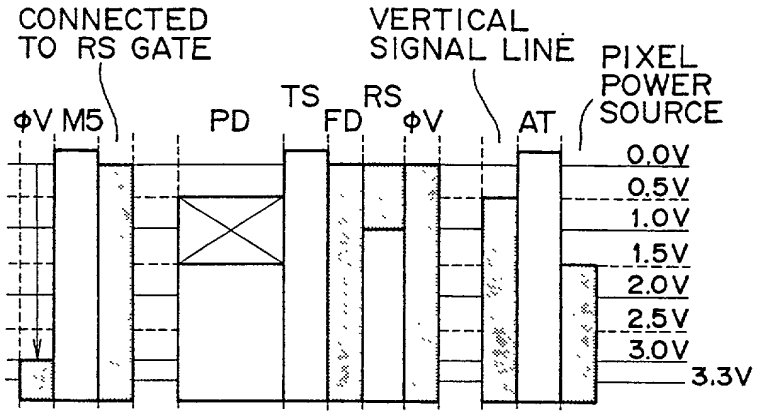


FIG. 16B t5<t<t6

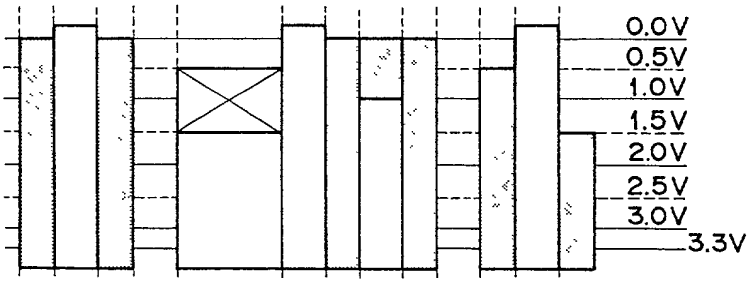


FIG. 16C t7<t

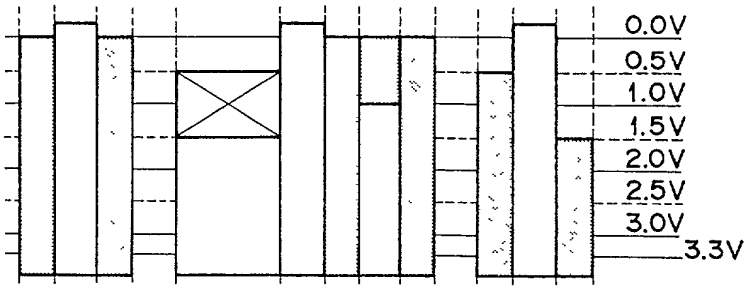


FIG. 17

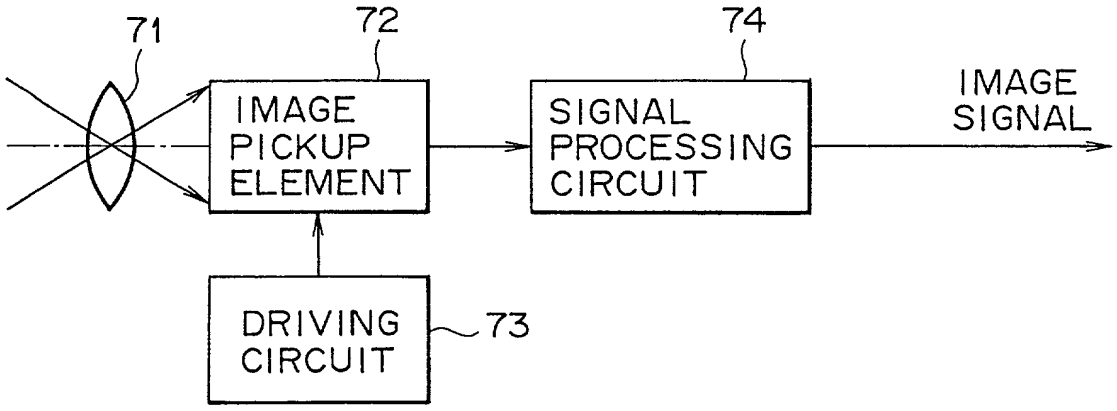
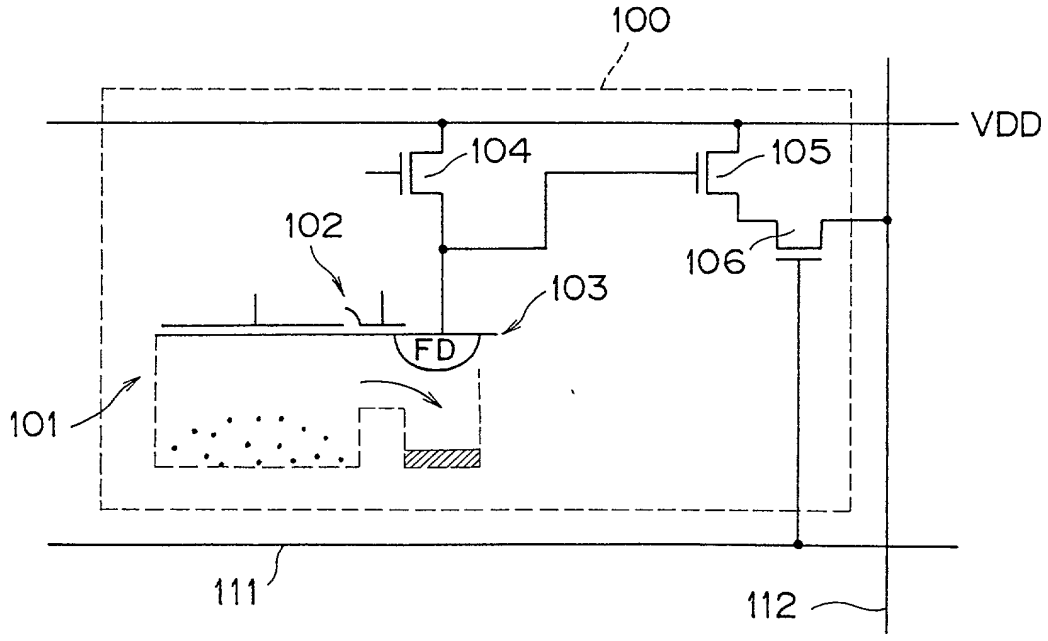

71
72
74
IMAGE PICKUP ELEMENT
SIGNAL PROCESSING CIRCUIT
IMAGE SIGNAL
DRIVING CIRCUIT
73

FIG. 18


100
VDD
104
105
102
106
103
FD
101
111
112

DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

SOLID-STATE IMAGING ELEMENT, METHOD FOR DRIVING THE SAME, AND CAMERA SYSTEM

Case No. ***P99.0401***, *the specification of which*

(check one)	X	is attached hereto.
	___	was filed on ____________________, as Application Serial No.____________________ and was amended on ____________________. (if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims as amended by any amendment referred to above.

I acknowledge the duty to disclose to the United States Patent Office all information which is known to me to be material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, 1.56(a).[1]

I do not know and do not believe this invention was ever known or used in the United States of America before my or our invention thereof, or patented or described in any printed publication in any country before my or our invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, and I believe that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months prior to this application, and that no application for patent or inventor's certificate on this invention has been filed in any country foreign to the United States of America prior to this application by me or my legal representatives or assigns, except as identified below:

I hereby claim foreign priority benefits under Title 35, United States Code, 119 of any foreign application(s) for patent or inventor's certificate listed below

Prior Foreign Application(s)

Number	Country	Date
P10-159050	Japan	June 8, 1998

---

[1] *(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made of record in the application, and*

(1) It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

(2) It refutes, or is inconsistent with, a position the applicant takes in:

(i) Opposing an argument of unpatentability relied on by the Office, or

(ii) Asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the above listed application on which priority is claimed:

Prior Foreign Application(s)

Number	*Country*	*Date*

If no priority is claimed, I have identified all foreign patent applications filed prior to this application:

Prior Foreign Application(s)

Number	*Country*	*Date*

And I hereby appoint Messrs. John D. Simpson (Registration No. 19,842), Dennis A. Gross (24,410), Robert M. Barrett, (30,142), Steven H. Noll (28,982), Kevin W. Guynn (29,927), Robert M. Ward (26,517), Brett A. Valiquet (27,841), Edward A. Lehman (22,312), David R. Metzger (32,919), Todd S. Parkhurst (26,494), James D. Hobart (24,149), Melvin A. Robinson (31,870), John R. Garrett (27,888), Paula J. Kelly (37,624), John W. Cornell (30,619), Robert J. Depke (37,607), Joseph P. Reagan (35,332), Michael R. Hull (35,902), Michael S. Leonard (37,557), William E. Vaughan (39,056), Lewis T. Steadman (17,074) and Marvin Moody (16,549) all members of the firm of Hill & Simpson, A Professional Corporation

Telephone: 312/876-0200 Ext. 3491

my attorneys with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith and direct that all correspondence be forwarded to:

Hill & Simpson
A Professional Corporation
85th Floor Sears Tower, Chicago, Illinois 60606

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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(if any) _____

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Residence _____
Citizenship _____
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Full name of sixth joint inventor,
(if any) _____

Inventor's signature _____ *Date* _____
Residence _____
Citizenship _____
Post Office Address _____
_____

Full name of seventh joint inventor,
(if any) _____

Inventor's signature _____ *Date* _____
Residence _____
Citizenship _____
Post Office Address _____
_____

Full name of eighth joint inventor,
(if any) _____

Inventor's signature _____ *Date* _____
Residence _____
Citizenship _____
Post Office Address _____
_____

Full name of ninth joint inventor,
(if any) _____

Inventor's signature _____ *Date* _____
Residence _____
Citizenship _____
Post Office Address _____
_____